Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC3037 DSP Architecture and Programming

Set A

Time : 3 hrs
Total Marks: 100

1. a. Discuss the advantages of Digital Signal Processing. (8 marks)

   b. Discuss the implementation aspects of FIR filters using single multiplier and accumulator hardware. (8 marks)

   c. Convolution is used to find (4 marks)

   i) Similarity between signals ii) Response of a system iii) Fourier Transform

   iv) Multiplication of Signals

OR

2. a. Explain with block diagram, the subband processing system that processes M subbands. (10 marks)

   b. Find the number of multiplications required to perform convolution of two sequencesof length 8 each by (i) direct method(ii) indirect method using FFT. (10 marks)

3. a) What is meant by Data path?Consider DSP5600x DSP processor and explain the design aspects of its data path with block diagram. (15 marks)

   b) Discuss the features of Multiplier in DSP5600 data path. (5 marks)

OR

4. a. Show how pipelining increases the throughput efficiency of a DSP processor.(8 marks)

   b. Write notes on Serial I/O. (6 marks)

   c. Bring out the difference between host port and communication port. (6 marks)

5. a. Draw the internal architecture of TMS320C5X CPU and explain each of its constituent functional blocks (CALU , PLU & ARAU) (14 marks)

   b.Discuss the features of Buffered Serial Port Interface and Time Division Multiplexed Serial Port Interface of TMS320C5X. (6 marks)

OR

6. 1. Explain the Register-indirect Addressing inTMS320C5X CPU with

   a. Modulo address arithmetic (5 marks)

   b. Bit Reversal (5 marks)

   c. Discuss the features, with Block diagram, of Buffered Serial Port Interface and Time Division Multiplexed Serial Port Interface of TMS320C5X. (10 marks)

7. a. Explain the differences in the architectural feature of TMS320C54X CPU from TMS320C5X CPU. (12 marks)

   b. Write short note on pipelining feature of TMS320C54X processor. (8 marks)

OR

8. a. Explain the Functional units in the Data Paths of TMS320C6x architecture (12 marks)

   b. Compare the TMS320C6x assembly programs to implement MAC operation with and without parallel instructions (8 marks)

9. a. Explain the ALU, MAC and Shifter sub units of ADSP-21xx architecture. (15 marks)

b. Discuss the use of Shadow register for Input and Output registers in each of thesubunits of ADSP-21xx processor. (5 marks)

Wishing you All the Best
